

DRS-LA413

Circuit Breaker Failure Relay

Operating Principle

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Operating Principle

DRS-LA413

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CAUTION

Installing, commissioning and operating of this product may be performed by thorough trained and

specialised personnel *

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- * **Definition:** <u>Specialised personnel</u>, when authorised and properly instructed, may perform following tasks:
- Installing, mounting, commissioning and operating of the apparatus and the system when familiar with.
- Maintenance and use of safety equipment according to standard rules and regulations.
- First Aid after extensive training.



1 General Description

The digital circuit breaker failure relay type DRS-LA413 is a member of the DRS-LIGHT series of the DRS-family (numerical protective relays). Therefore the following descriptions should be known in addition:

DRS-LIGHT, Operation Manual DRS-LIGHT, Local Operation via Keypad and Display DRS-WIN, Software Manual

The circuit breaker failure protection provides a backup protection in the case, that the local circuit breaker fails to clear a system fault. So a retrip signal to the local circuit breaker and/or a trip signal to a higher levelled circuit breaker is issued to terminate the failure.

A single or a three pole breaker failure detection with different pick up signals and time delays is provided. Additional features include an event recorder, a fault recorder with FFT analysing tool and the possibility for the simulation of binary inputs for testing purposes.

The usage of digital signal processing, self monitoring and communication capabilities increases the reliability and availability.

All included protection functions, that are available:

- circuit breaker failure protection
- definite time overcurrent
- signal function, sf1
- signal function, sf2
- signal function, sf3
- signal function, sf4

2 Functional Description

The breaker failure protection function evaluates, whether the local circuit breaker has fully opened and cleared a fault in the event of an external trip signal. If this requirement is not fulfilled (case of a circuit breaker failure), a current still flows through the breaker poles and a backup trip signal will be issued to interrupt the fault current. In addition to the current detector a mechanical signal can be used for supervision.

According to the logic diagram, the circuit breaker failure protection can be initiated in two independent ways (per phase):

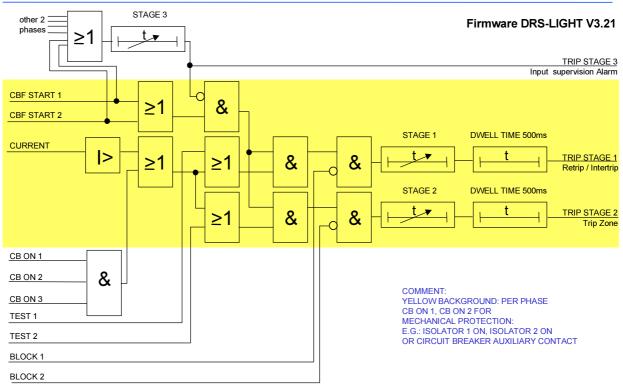
- CBF Start 1
- CBF Start 2

Both starters are able to be assigned to either an external or internal signal by a software matrix. For example the integrated O/C function trip can be used as internal starter, an external protective device serves for an external trip signal.



Two conditions are established for the detection of a breaker failure:

- Measurement, whether the current in one phase exceeds a set threshold value still after the external trip signal (monitoring the current through the breaker poles).
- Additionally there are protection functions which have no current criterion for a trip. So the
 monitoring of the breaker poles current is not relevant. Such functions are: Buchholz
 protection, oil pressure protection, temperature protection, overvoltage protection, and so on.
 Therefore the position of the circuit breaker auxiliary contact is monitored (inputs CB ON in
 the logic diagram). For this case the output of the circuit breaker auxiliary contact has to be
 connected to a binary input of the relay.



Logic of Circuit Breaker Failure Protection (50BF)

figure 1: logic diagram of the circuit breaker failure protection function

As it can be seen in figure 1 the two criterions described above are combined with an OR logic. So only one has to be fulfilled. In case of an initiation with one of the CBF Start Signals (AND logic between CBF initiation and criterions for CBF detection), a trip impulse with a dwell time of 500 ms is issued (via an output contact) after an adjustable time delay. The dwell time ensures a sufficient length for the trip impulse that the circuit breaker can fully open. Note: the value of the dwell time is independent of the setting of the time delay.

Further two trip stages exists (stage 1 and stage 2), each adjustable with the mentioned time delay. Both time delays will be started simultaneously in the event of a pick up. In example stage 1 can be used to send a retrip signal to the local circuit breaker or an intertrip signal to i.e. a line protection relay.



If the circuit breaker failure condition is still set after the execution of stage 1, the second stage issues (after the time delay) a trip signal for example to a higher levelled circuit breaker to clear the fault.

The circuit breaker failure start signals not only initiate the trip stages 1 and 2, but they also start the supervision stage 3. After a settable time delay it clears the picked up stages 1 and 2 and issues the so-called "input supervision alarm" signal. Stage 3 prevents that the circuit breaker failure protection function is always initiated by the start signals, for example in case of external wiring or contact failure. Maltrips can be avoided.

The CBF function also includes a test input and a blocking input for each of the trip stages. By setting the test input it is possible to check the correct execution of the function. But figure 1 shows, that the CBF start signals also have to be set for this purpose (AND logic). Depending on the setting of the blocking inputs it results in a blocking of stage 1, stage 2 or both stages.

3 Application Guide

In the following typical applications for the circuit breaker failure relay are described. In addition some figures show the necessary settings under operation software DRS-WIN.

3.1 Example 1: Single phase initiation

The circuit breaker failure relay caters for the application, that a single pole initiation (phase separated initiation) of the function has to be provided. In this case the CBF start signals are carried out for each phase from an external protection device, which is in example an overcurrent relay and are connected to binary inputs of the CBF relay (binary input 1 to input 3).

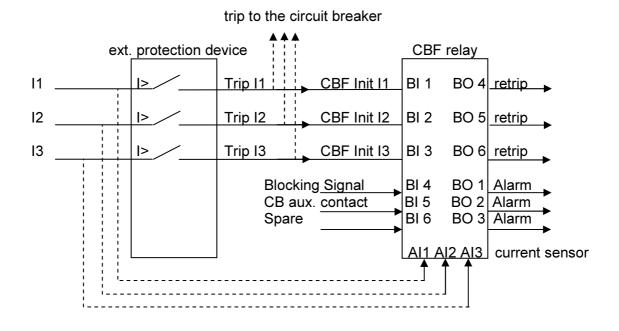


figure 2: block diagram of the phase separated initiation



As mentioned above, in case of a circuit breaker failure a current still flows through the breaker poles after sending a trip signal. This current level and the trip signal of one phase, which is the CBF initiation signal, pick up the CBF relay and a backup trip signal will be issued after a chosen time delay to interrupt the fault current. For security reasons it is recommended, that the fourth binary input is used for a blocking signal. So it is possible to control the release of the function. In addition a mechanical protection is applicable by monitoring the circuit breaker auxiliary contact (binary input 5).

The necessary settings under DRS-WIN are shown in figure 3. It includes the "Protective function inputs" – window. For this example a function blocking via the binary input 4 is used. Considering the mechanical protection, the signal of binary input 5 has to be set to the corresponding inputs CB On (1 to 3; Refer to the logical AND connection of these 3 signals). The single pole initiation signals (binary input 1 to 3) are used for the corresponding phases.

🔚 [1A45] CBF LA471:3		X
Protective function inputs CBF		
Current inputs	<u> </u>	Blocking inputs
[Al.01] I1	Phase A Stage 1	(BI.04) CBF Blocking
[AI.02] 12	Phase B Stage 2	(BI.04) CBF Blocking
[AI.03] 13 🔹 🛶	Phase C	Test inputs
p	Stage 1	Unused 🗾
	Stage 2	Unused 🔽
		Auxiliary inputs
	A CBF Start 1	(BI.01) CBF Init I1
	A CBF Start 2	Unused 🔽
	B CBF Start 1	← [BI.02] CBF Init 12
	B CBF Start 2	Unused
	C CBF Start 1	[BI.03] CBF Init I3
	C CBF Start 2	Unused
	CB On 1	(BI.05) CB Aux. Contact
	CB On 2	(BI.05) CB Aux. Contact
	CB On 3	(BI.05) CB Aux. Contact

figure 3: Setting under DRS-WIN for CBF phase separated initiation

Further it can be seen, that the initiation input 2 (CBF Start 2) is not used. In addition an internal CBF start can be achieved by using a virtual input, which will be set via an internal protection function (i.e. overcurrent function). This virtual input is the second start signal (equal for all three phases).

The allocation of the software trip outputs to the hardware device outputs is done via the "Trip Matrix" under DRS-WIN. The DRS-LIGHT provides in total 10 outputs. As shown in figure 2, binary outputs 4 to 6 are used for the retrip/intertrip signal (single pole). Further outputs 1 to 3 are used to issue alarm signals. But they could also be used for a trip signal to other circuit breakers. The software "Trip Matrix" is very flexible.



3.2 Example 2: Three phase initiation

In HV-systems often only three pole circuit breakers are applicable and therefore a common phase initiation of the CBF has to be provided. The relay also caters this case. The principle of the CBF detection is the same as in example 1 or explained in the functional description (current level detector or mechanical protection). Figure 4 shows a sketch of the connection diagram (only an example). The relay is hard wired with the circuit breaker. So the CBF initiation is carried out directly from the circuit breaker with only one signal for all three phases (read in with binary input 1).

For security reasons it is also for this example recommended to control the release of the CBF relay with a blocking signal (binary input 4). It helps to prevent maltrips. Binary input 2 could be used for the mechanical protection, e.g. Buchholz protection and transformer winding temperature protection. According to the logical AND connection, it is possible to combine the Buchholz protection with the circuit breaker auxiliary contact.

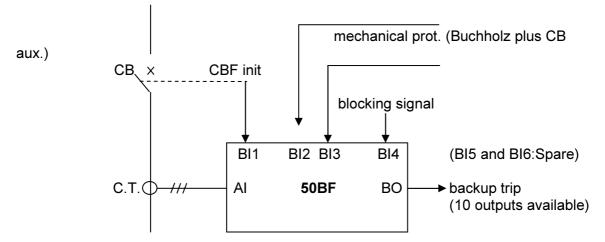


figure 4: connection diagram of a CBF three pole initiation

The corresponding setting under DRS-WIN is shown in figure 5.

[M681] CBF Test File:3		
Protective function inputs CBF		
Curent inputs		Blocking inputs
[Al.01] I1	Phase A Stage 1	EI.04] CBF blocking
[AI.02] 12	Phase B Stage 2	(BI.04) CBF blocking
[AI.03] 13 🗨 🛶	Phase C	Test inputs
	Stage 1	Not used
	Stage 2	← Not used 🔹
		Auxiliary inputs
	A CBF Start 1	EI.01] CBF init
	A CBF Start 2	← Not used 🔽
	B CBF Start 1	(BI.01) CBF init
	B CBF Start 2	← Not used
	C CBF Start 1	(BI.01) CBF init
	C CBF Start 2	← Not used
	CB On 1	(BI.02) Buchholz prot.
	CB On 2	[BI.02] Buchholz prot.
	CB On 3	EI.03] CB aux. contact

figure 5: Setting under DRS-WIN for CBF common phase initiation



The three pole initiation signal (binary input 1) is used for all phases. CB On1 and CB On2 are fed with the mechanical transformer protection signals (also CB On3 to consider the logical AND connection). The signal of binary input 4 controls the release of the function.

3.3 Example 3

With reference to application example 2, it should be mentioned that it is also possible to work with one CBF initiation signal for three phases and three separate inputs for the mechanical protection. Compared with figure 5, binary input 4 has to be used for CB On3. Please note, that the three input signals CB On 1,2,3 are logically AND connected (see fig.1).

3.4 Hints:

Using the LED Matrix under DRS-WIN, it is possible to connect the output of Stage 3 (input supervision alarm) with a LED. This causes an indication of the supervision alarm.

Using the Trip Matrix under DRS-WIN, the trips of the CBF function of each phase not only can be combined with an output contact, but also with a virtual output. This provides an easier allocation in the event and fault recording.

4 Connection Diagram of the DRS-LIGHT LA4:

A typical connection diagram of the DRS-LIGHT, hardware type DRS-LA4XX is shown in figure 6.

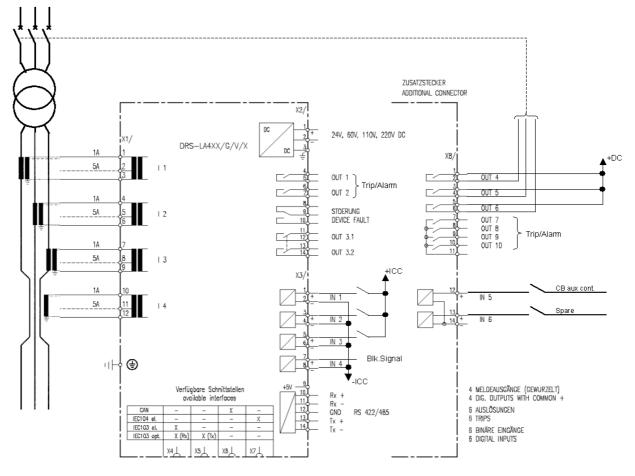


figure 6: connection diagram of the DRS-LA4XX



5 Performance Specification

Technical Data

Auxiliary supply	240, 220, 110, 60, 24 VDC	
	approx. 10 W	
Analogue Inputs	4 CTs; 1A or 5A	
Nominal frequencies	50; 60; 16.7 Hz	
Trip/LED Matrix	integrated software matrix	
Interface	RS485	
	optional IEC 60870-5-103	
Binary inputs	6 free programmable	
Binary outputs	10 trip-/alarm relays,	
	1 internal fault, 8 LEDs	
local operation	6 keys, 2x16 digit LCD	

Setting Level

Setting range	0.10 to 5.00 A
	in steps 0.05 A
Operate accuracy	±5.0% or ±20mA
Reset accuracy	=85% of operate value
Repeatability	±3%

Setting Delay

ootang bolay	
Setting range	0.01 to 1.00 s
	in steps 0.01 s
Delay accuracy	±1.0% or 2 ms
Reset time	=15 ms
Repeatability	±1%

Current Inputs

e an encinpace	
Current Level	Time
4xI _N	continuous
10xI _N	30s
100xI _N	1s
250xl _N	1 half cycle

Burden <0.1 VA at I_N

Binary Inputs

Input voltages V _H	220, 110, 60, 24 VDC
current consumption	2.5 – 3 mA
operation value	approx. 0.7 x V _H

Binary Outputs

Binary Galpalo	
Contact voltage	max. 250 VDC
Trip contact	continuous current 8A
mechanical live duration	5x10 ⁷ switching cycles



Tests

EN 50263
IEC 60255 part 25
IEC 60255 part 22-1, Class 3
IEC 60255 part 22-2, Class 4
IEC 60255 part 22-3
IEC 60255 part 22-4, Class 4
IEC 61000-4-5; Class 3
IEC 60255 part 21-1,-2
IEC 61000-4-6
IEC 61000-4-8; Class 4
IEC 60255-5; 5kV

Case data

Protection type	IP51
Mounting	Panel flush or projection mounting, 19", 6U height / 21U width
Dimensions in mm	H x W x D: 243 x 96 x 208
Weight	Approx. 3 – 4 kg

6 **Relay Settings**

Selection ('OK' key from main menu) These settings allow each function provided in the relay to be enabled or disabled

Setting	Range (default)
Overcur. 3-ph.2-st.	Active, Not active
3-phase overcurrent 2 definite-time stages	
CBF	
circuit breaker fail	
Signal Function 1	
timer function	
Signal Function 1	
timer function	
Signal Function 1	
timer function	
Signal Function 1	
timer function	

Overcur. 3-ph.2-st.

Setting	<u>Range (default)</u>
Operate Value St.1	0.30, 0.35… 1.20 …5.00 A
3-phase overcurrent stage 1 current operate level	

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Time Delay St.1	0.00, 0.05 3.00 10.00 s
3-phase overcurrent stage 1 definite-time delay	
Operate Value St.2	0.30, 0.35 5.00 30.00 A
3-phase overcurrent stage 2 current operate level	
Time Delay St.2	0.00, 0.05 1.00 10.00 s
3-phase overcurrent stage 2 definite-time delay	

CBF

Setting	Range (default)
I> CBF	0.10, 0.15 0.30 5.00 A
Circuit breaker fail current setting	
t> CBF Trip Feeder	0.01, 0.02 0.20 1.00 s
Circuit breaker fail retrip (feeder) (stage 1) time setting	
t> CBF Trip Zone	0.01, 0.02… 0.50 …1.00 s
Circuit breaker fail (backtrip) (zone) (stage 2) time setting	
CBF Start Superv.	1, 2 5 180 s
Circuit breaker fail alarm time (stage 3) setting	

Signal Function 1

Setting	<u>Range (default)</u>
Time Delay	0.00 , 0.0510.00 s
The delay before an output occurs	
Active Edge	Rising, Trailing
Set 'Rising' to start the timer on a low-high transition; set 'Trailing' to start the timer on a high-low transition	



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Our address:		
ANDRITZ HYDRO GmbH Dpt. PRT Wienerbergstr. 41 D	Phone: Fax:	++43 1 81195 Ext. 6936 ++43 1 81195 Ext. 6951
A-1120 VIENNA AUSTRIA	E-mail:	martin.hantsch@andritz.com http://www.andritz-hydro.com/



То

ANDRITZ HYDRO GmbH Dpt. PRT / attn. Mr. Hantsch Wienerbergstr. 41 D A-1120 VIENNA

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